a second dopant implant in only the capacitor contact region, the second dopant implant aligned with the insulating spacer extending over the capacitor contact region such that substantially all of the second dopant implant is formed in only that portion of the capacitor contact region not covered by the insulating spacer.

27.(amended once) A semiconductor memory device, comprising:

a silicon structure having a first conductivity type;

a gate electrode over the silicon structure having a first conductivity type;

a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;

a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;

a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type;

insulating spacers extending along the sidewalls of the gate electrode and over a portion of the first dopant implant in the capacitor and bit line contact regions;

a second dopant implant in only the capacitor contact region, the second dopant implant aligned with the insulating spacer extending over the capacitor contact region such that substantially all of the second dopant implant is formed in only that portion of the capacitor contact region not covered by the insulating spacer;

a capacitor first conductor in electrical contact with the capacitor contact region;

a dielectric over the capacitor first conductor; and

a capacitor second conductor over the dielectric.

28.(amended once) A semiconductor memory device, comprising:

a silicon structure having a first conductivity type;

a gate electrode over the silicon structure;

a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;

a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;